REMARKS

Claims 1-16, and 18-58 are present in this application. Claims 1-15 and 39-57 have been withdrawn. Of the examined claims, claims 16, 28 and 37 are independent claims.

In view of the above amendment, applicant believes the pending application is in condition for allowance.

Allowable Subject Matter

Applicants thank the Examiner for indicating that claims 28 and 37 contain allowable subject matter. Accordingly, claims 28 and 37 have been re-written into independent form. Applicants respectfully request that claims 28 and 37 be allowed.

In addition, it is noted that claim 22 had previously been indicated as allowable, as well. Claim 22 is listed in the rejection based on Yudasaka, but no reasons have been presented in the body of the rejection. Applicants submit that Yudasaka fails to teach the features recited in claim 22, and respectfully request that the claim be reconsidered and reinstated as being allowable.

Claim Rejection under 35 USC 102(b) – Yudasaka

Claims 16, 18-24, 29-34, and 58 have been rejected under 35 U.S.C. 102(b) as being anticipated by JP 06-011729 (Yudasaka). Applicants respectfully traverse this rejection.

Summary of Claimed Subject Matter

Claim 16 covers embodiments of the present invention that are directed to a semiconductor device in which a single-crystal silicon thin film device is bonded to an insulating substrate (without an adhesive), consisting of a non-single-crystal thin film device. In an example embodiment, the single-crystal thin film device is bonded to the insulating substrate before the non-single-crystal thin film device is formed (Fig. 1). In another example embodiment, the non-single-crystal thin film device is formed before the single-crystal thin-film device is bonded (Fig. 2). In each case, an interlayer insulating film 4 is formed as a step between the formation of the thin film layers. In the embodiment shown in Fig. 1, the single-crystal thin film device is bonded (Fig. 1(c)), followed by formation of an interlayer insulating film 4 (Fig. 1(d)), then forming the polycrystalline layer 5' (Figs. 1(e), 1(f)). In the embodiment

shown in Fig. 2, polycrystalline layer 5' is first formed (Figs. 2(b), 2(c)), then an interlayer insulating film 4 is formed (Fig. 2(d)), followed by bonding of the single-crystal thin-film device 10a (Figs. 2(e), 2(f)). Embodiments in Figs. 3, 4, and 6 follow a similar sequence of steps. In the case of the embodiment in Fig. 6, an amorphous island 63/64 is formed as the non-single-crystal thin-film layer over an interlayer insulating film 61. Thus, in each case the lower surface of the single-crystal silicon thin-film 14a/14b is formed at a different height than the non-single-crystal silicon thin film 5'/63,64, based in part on the order of forming the film layers relative to the interlayer insulating film 4/61.

Yudasaka

Yudasaka discloses a liquid crystal display device that appears to show the general concept of forming both single crystal silicon films 202, 203 and a polycrystalline silicon film or non-crystalline silicon film 204 formed on an insulating substrate 201. However, Yudasaka does not appear to realize problems that can occur in manufacturing such a semiconductor device. For example, Yudasaka does not appear to solve problems with bonding and stripping of the silicon thin film.

Differences

The present invention solves problems associate with manufacturing a semiconductor device having both a single-crystal silicon thin film and a non-single crystal silicon thin film formed in different areas of an insulating substrate. Manufacturing methods disclosed in the present application result in a structure in which a bottom surface of the non-single-crystal silicon thin film and a bottom surface of the single-crystal silicon thin film are at different heights relative to the insulating substrate (e.g., the embodiments shown in Figs. 1, 2, 3, 4, and 6). Applicants submit that Yudasaka discloses a manufacturing method in which both a single-crystal silicon thin film and a non-single-crystal silicon thin film are disclosed as being formed on a common surface at the same height above the insulating substrate.

In order to clarify that the present invention is a product formed by a different manufacturing process, claim 16 has been amended to include the feature that a nearest surface

of the non-single-crystal silicon thin film and a nearest surface of the single-crystal silicon thin film are at different heights above to the insulating substrate. Applicants submit that Yudasaka does not show this resulting structure.

Applicants request that the rejection be reconsidered and withdrawn.

Claim Rejection under 35 USC 102(b) – Spitzer

Claims 16, 18-21, 23-27, 29-34 and 58 have been rejected under 35 U.S.C. 102(b) as being anticipated by WO/93/15589 (Spitzer). Claims 35, 36, and 38 have been rejected based on the combination of Spitzer and Okabe. Applicants respectfully traverse these rejections.

At the outset, page 52 of Spitzer that is primarily relied on for teaching the features recited in the above-stated claims, contains a statement that, "[t]he starting structure is a silicon wafer 718 upon which an oxide layer 716 and a thin film of poly-si, a-si, or x-si 714 is formed ..." Also, Spitzer's Fig. 25 has been alleged to show wafers A, B, and C on the same glass substrate 712.

Applicants submit that it is clear that this statement applies to a "starting structure," i.e. intermediate product, and provides a material for the thin film in the alternative, "or." Fig. 25 clearly shows standard drawing features of a jagged line to indicate a continuation of a same wafer and a solid line to indicate ends of the wafer. Also, Spitzer clearly describes three wafers A, B, and C, instead of a single wafer A. Thus, Applicants submit that there is simply no basis in fact for an assertion that the three wafers A, B, and C of Fig. 25A have different types of thin films formed thereon, much less that wafers A, B, and C are the same wafer with devices having both poly-Si/a-Si/x-Si and single-crystal crystal silicon thin films, and respective devices, formed thereon.

Therefore, evidence provided only indicates that assertions made in the Office Action come from knowledge gleaned only from applicants' own disclosure, and constitutes impermissible hindsight reasoning. (M.P.E.P. § 2145 X.A.).

Furthermore, the ISE and CLEFT processes mentioned on page 52 of Spitzer were known methods of obtaining single crystal silicon from polycrystalline or amorphous silicon. Preparation of single crystal silicon films using these processes are described, for example, on

pages 21-23 of Spitzer. Applicants submit that one of ordinary skill in the art would understand that Spitzer at pages 52-53 teaches a process that results in single crystal silicon devices formed on glass substrates.

In addition, Applicant submits that Fig. 25 of Spitzer does not show at least the claimed feature of a nearest surface of the non-single-crystal silicon thin film and a nearest surface of the single-crystal silicon thin film are at different heights above to the insulating substrate.

These arguments apply as well to dependent claims 35, 36, and 38.

Applicants request that the rejections be reconsidered and withdrawn.

Conclusion

In view of the above remarks, it is believed that claims are allowable.

Should there be any outstanding matters that need to be resolved in the present application, the Examiner is respectfully requested to contact **Robert Downs** Reg. No. 48,222 at the telephone number of the undersigned below, to conduct an interview in an effort to expedite prosecution in connection with the present application.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies to charge payment or credit any overpayment to Deposit Account No. 02-2448 for any additional fees required under 37.C.F.R. §§1.16 or 1.14; particularly, extension of time fees.

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Respectfully submitted,

By Robert Downs #48,222

Charles Gorenstein
Registration No.: 29,271
BIRCH, STEWART, KOLASCH & BIRCH, LLP
8110 Gatehouse Road
Suite 100 East
P.O. Box 747
Falls Church, Virginia 22040-0747
(703) 205-8000
Attorney for Applicant